REMARKS

The application contains claims 1-7, 9-20, and 22-37. Claims 4-7 and 9-15 are allowed. Claims 17-19 are identified as allowable. Some claims have been amended for form; none were amended for reasons of patentability. In view of the foregoing amendments and following remarks, Applicants respectfully request allowance of the application.

Applicants thank Dr. Tsai for the courtesy of the March 30 interview with the undersigned. At that meeting, Applicants' representative presented arguments in rebuttal of the rejections made in the February 24, 2004 Office Action. These arguments are repeated in this response.

THE SECTION 101 REJECTIONS SHOULD BE WITHDRAWN

Claims 1-3, 20 and 22-27 stand rejected as non-statutory under 35 U.S.C. § 101. Applicants respectfully request withdrawal of the outstanding rejections because the claims clearly define patentable subject matter.

The Office Action essentially makes three arguments in favor of its section 101 rejection:

- a memory can be defined as a device or space where information can be stored and retrieved, such as the pages of a book,
- the claims are not tangibly embodied on a computer readable medium, and
- the claims define non-statutory subject matter because the claims fail to recite the necessary functional interrelationship within the architecture to constitute a data structure.

Applicants respectfully submit that these grounds do not provide sufficient basis to reject the pending claims. A claim defines statutory subject matter if it describes an invention that produces a useful, concrete and tangible result. MPEP § 2106 (p. 2100-6). Here, the rejected claims satisfy this requirement.

Claims 1-3, 20 and 22-27 are apparatus claims. They recite:

> a memory entry to store a trace having a multiple-entry, single exit architecture [claim 1].
>
> comprising a memory entry to store a sequence of program instructions as a trace, the instructions defining a program flow that progresses from any

instruction therein to a last instruction in the memory entry and in which the trace has multiple separate prefixes [claim 20].

A memory comprising storage for a plurality of traces and means for indexing the traces by an address of a last instruction therein according to program flow [claim 23].

These claims expressly recite tangible apparatus – memory entries and storage – and also recite functional data structures stored therein. Claim 1, for example, recites storage of a trace which has a multiple-entry, single exit architecture. Claim 20 recites a trace that defines program flow that progresses from any instruction therein to a last instruction in the entry. Claim 20 also recites a trace that has multiple prefixes. Finally, claim 23 recites a means for indexing traces by an address of a last instruction therein.

The specification explains that these inventions define useful subject matter. As compared to traditional traces, the claimed inventions provide an architecture that contributes to reduced redundancy when stored in a cache. They permit multiple entry points whereas a traditional trace permits only one entry point. Further, they permit dynamic extension of the traces to include additional instructions (see FIG. 4 (b)). See, specification at page 3. Not only do these claims refer to statutory apparatus (a memory), these inventions clearly define inventions that produce useful, concrete and tangible results. The claims clearly are statutory under 35 U.S.C. § 101.

The Office Action's stated reasons for rejecting the claims are inappropriate under a § 101 analysis as shown below:

OFFICE ACTION'S REASONING	RESPONSE
a memory can be defined as a device or space where information can be stored and retrieved, such as the pages of a book,	Even if the Examiner were correct, printed pages of a book are statutory subject matter. It is a tangible invention under § 101.
the claims are not tangibly embodied on a computer readable medium, and	Incorrect. The claims refer to "memory entries" and "storage," which are computer readable media. Applicants note that § 101 does not require express recitation of a computer readable medium, only an invention that produces a useful, concrete and tangible result.
the claims define non-statutory subject matter because the claims fail to recite the necessary functional interrelationship within the architecture to constitute a data structure.	Functional relationships are sufficient, but not required, to define statutory subject matter. Here, claims 1, 20 and 23 define features of the invention that provide the advantages noted above: reduced redundancy when stored, dynamic extension and multiple entry points. Interestingly, traditional traces do not possess these advantages.

Applicant respectfully suggests that the claims as currently written satisfy all requirements of 35 U.S.C. § 101.

THE CLAIMS DEFINE OVER THE ART.

Claims 1-3, 16, 20 and 22-27 stand rejected as anticipated by Agarwal, U.S.P. 5,966,541. Applicants respectfully request withdrawal of these rejections because Agarwal does not teach all elements of the pending claims.

Consider claim 1, which recites:

> Apparatus, comprising a memory entry storing a trace having a multiple-entry, single exit architecture.

Agarwal does not teach such subject matter. Agarwal's FIG. 8, which is cited by the Office Action, provides a generic representation of program flow. Agarwal does not describe any relationship between the program flow and memory. Agarwal does not explain which portions of this program flow are stored in a common entry or, for example, which portions might be stored across multiple entries. Agarwal's "blocks" 100, 101, 102 and 103 each have a single entry, single exit architecture. Accordingly, claim 1 distinguishes over this reference.

Claim 2 recites that a trace has multiple independent prefixes and a common shared suffix. Agarwal discloses nothing of the sort. The Office Action argues that blocks 101 and 102 could be considered prefixes to a common suffix (block 103), but there is no teaching in the reference from which to draw such a conclusion. There is absolutely no disclosure to suggest that blocks 101-103 are stored in a common memory entry as recited in this claim. Claim 2 also distinguishes over this reference.

Claim 3 recites that the entry is indexed by an address of a terminal instruction therein. Agarwal does not disclose this subject matter. The Office Action does not assert that it does; instead, it argues that such subject matter is inherent. Applicants respectfully disagree. As described in the interview, traces normally index the instructions by the first instruction therein, not the terminal instruction as proposed by claim 3. Agarwal's system also could index the instructions by the address of the first instruction in his blocks, not the terminal instruction. Claim 3 is not rendered inherent by Agarwal. Claim 3 also defines over the art.

Claim 16 is an independent claim which recites:

a front end stage to store blocks of instructions in a multiple-entry, single exit architecture when considered according to program flow, and

Agarwal does not disclose such subject matter. As noted, Agarwal's blocks are a single-entry, single exit architecture. The Office Action actually considers Agarwal's individual blocks 101-103 as a "super-block" of some kind. Applicants respectfully suggest that this is inappropriate. Agarwal has no disclosure to suggest that his blocks should be interpreted in such a manner. Instead, Agarwal very clearly illustrates the nature and character of his block. The Office Action's analysis directly contradicts an express teaching of the prior art and provides no justification for doing so. Applicants respectfully submit this is improper. Claim 16 defines over this art.

Claim 20 recites:

Apparatus, comprising a memory entry storing a sequence of program instructions as a trace, the instructions defining a program flow that progresses from any instruction therein to a last instruction in the memory entry and in which the trace has multiple separate prefixes.

Agarwal does not disclose this subject matter. As noted, Agarwal has no disclosure that relate memory entries to the structure of a trace; any inference to the contrary is based on pure conjecture. Further, Agarwal discloses only abstract blocks, each of which has a single-entry, single-exit structure. None of his blocks contains multiple separate prefixes. Again, the Office Action merely speculates that Agarwal's disclosure of a plurality of blocks should instead be considered a single block, despite clear teachings from Agarwal to the contrary. Claim 20 defines over this art.

Claim 22 recites:

wherein the memory entry is indexed by an address of a terminal instruction therein.

Agarwal discloses no such subject matter and does not render it inherent. Agarwal does not disclose any indexing scheme for the blocks of FIG. 8. The blocks could be indexed by the first instruction in the block instead of the terminal instruction. One cannot tell from Agarwal's disclosure. Accordingly, Agarwal does not render claim 22 inherent.

All pending claims recite statutory subject matter that define over the cited art. Accordingly, Applicants respectfully request allowance of the application.

Respectfully submitted,

Date: 4/8/04

Robert L. Hails, Jr.
Registration No. 39,702
(Attorney for Intel Corporation)

ATTORNEYS FOR INTEL CORPORATION

KENYON & KENYON
1500 K Street, N.W.
Washington, D.C. 20005
Ph.: (202) 220-4200
Fax.: (202) 220-4201